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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/081,375 | 02/22/2002 | Kevin M. Conley | M-11604 US | 9646 |

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| EXAMINER | |
|---|---|
| LANE, JOHN A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2188 | 6 |

DATE MAILED: 07/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/081,375 | CONLEY ET AL. | |
| | Examiner | Art Unit | |
| | Jack A Lane | 2188 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4+5
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This Office action is responsive to the application filed 02/22/02. Claims 1-28 are presented for examination. In response to this Office action, please insert the corresponding U.S. patent numbers of the U.S patent applications found in the specification. Applicant should carefully review related U.S. patent No.'s 6,349,056, 6,426,893 and 6,570,785 for double patenting issues with the present set of claims. For example, claims 6 and 16 of the present specification and claims 1-9 of patent 6,349,056 (as discussed on page 17 of the present specification) recite a RAM memory section connected to store a copy of the data transferred into the data register." Claims 13-15, 17, 18, 20-25, 27 and 28 of the present specification and various claims of the 6,426,893 and 6,349,056 patents appear to recite similar programming and erasing functions. Applicant should note any double patenting rejection can be rendered moot by amending claims to overcome the primary reference to Araki et al. That is, there does not appear to a double patenting issue between the prior patents and the main invention found in the independent claims.

2. The examiner requests, in response to this Office action, any reference(s) known to qualify as prior art under 35 U.S.C. sections 102 or 103 with respect to the instant claims. That is, any prior art (including any products for sale) similar to

the instant claimed invention that could reasonably be used in a 102 or 103 rejection. This request does not require applicant to perform a search. This **request** is not intended to interfere with or go beyond that **required** under 37 C.F.R. 1.56 or 1.105. This request may be fulfilled by asking the attorney(s) of record handling prosecution and the inventor(s)/assignee for references qualifying as prior art. A simple statement that the query has been made and no prior art found is sufficient to fulfill the request. Otherwise, the fee and certification requirements of 37 CFR section 1.97 are waived for those documents submitted in reply to this request. This waiver extends only to those documents within the scope of this request under 37 CFR, section 1.105 that are included in the application's first complete communication responding to this requirement. Any supplemental replies subsequent to the first communication responding to this request and any information disclosures beyond the scope of this request under 37 CFR section 1.105 are subject to the fee and certification requirements of 37 CFR section 1.97. In the event prior art documentation is submitted a discussion of relevant passages, figs. etc. is requested. **A response to this inquiry is greatly appreciated.**

The examiner also requests, in response to this Office action, support be shown for language added to the claims on amendment. That is, indicate support for newly added claim language by specifically pointing to page(s) and line no(s).

in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1-5, 8, 10, 12, 19 and 26 are rejected under 35 U.S.C. § 102(e) as being anticipated by Araki et al. (Pat. No. 6,525,952).

Araki et al. teaches the claimed controller as circuitry including control block 11 and flash buffers BFO shown in figures 2 and 3. The claimed "memory comprising a plurality of independently controllable non-volatile data storage sections" corresponds to flash memory 7 shown in figure 2. The claimed function of "data is transferable from the controller to a second of the data storage sections while data is being programmed into a first data storage of the data storage sections" corresponds to the function discussed at col. 9, lines 50-60 and shown in figure 8. In steps S3 and S4 of the flow chart of figure 8, a sector 0 is written into one storage section in flash memory 7 from an associated flash buffer in parallel

with sending sector 1 from the page buffer to a different flash buffer associated with a different section of flash memory. The claimed "first and second data buffer" correspond flash buffers BFO.

As per claim 4, the claimed "each storage sections comprises a data register" corresponds to flash buffers BF.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103 (a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 U.S.C. § 102(f) or (g) prior art under 35 U.S.C. § 103(a).

6. Claim 3 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Araki et al. (Pat. No. 6,525,952) in view of Katayama et al. (6,317,371).

Araki teaches the invention substantially as claimed as discussed above in section 4. However, Araki teaches a single page buffer in control block 11. Claim 3 calls for the controller to have first and second data buffers. Katayama is introduced as teaching 2 data buffers in a control section 51 as shown in figure 6. The data buffers provide improvements in processing performance and reliability.

Because multiple data buffers provide for improvements in processing performance and reliability, it would have been obvious to use plural buffers in the device of Araki to receive and store multiple portions of data for programming in the memory. Therefore, the claimed invention would have been obvious to one of ordinary skill in the art at the time of the invention.

7. Claim 6 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Araki et al. (Pat. No. 6,525,952) in view of Conley et al. (6,349,056).

Araki teaches the invention substantially as claimed as discussed above in section 4. However, the claimed "RAM memory section connected to store a copy of the data transferred into the data register" is not discussed.

The related patent to Conley teaches a RAM memory for storing a copy of the data transferred (as discussed on page 17 of the present specification) for improving reliability during program verification.

Because a copy of programmed data for comparison to programmed data improves reliability, it would have been obvious to use a RAM memory in the device of Araki to store copy data and verify the program function. Therefore, the claimed invention would have been obvious to one of ordinary skill in the art at the time of the invention.

8. Claims 7, 9, 11, 13-18, 20-25 and 27-28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Araki et al. (Pat. No. 6,525,952) in view of Conley et al. (6,426,0893) and Mangan et al. (6,570,785).

Araki teaches the invention substantially as claimed as discussed above in section 4. However, various well known programming and erasing functions are not discussed in Araki. Applicant should consider the programming and erasing functions discussed in the present specification and the related patents. The examiner believes most, if-not-all, dependent claim features related to programming and/or erasing are taught by Conley and Mangan. However, in the event a claim feature is not expressly or inherently taught by the references applicant should consider the claim features in light of the Official notification put forth below.

Official notice is taken of the prior art teaching any claim feature not specifically shown in the references. That is, any prior art (including that of record) teaching the more well known claim features commonly found in the

dependent claims. The claim features, while part of the invention, appear to be well known and their relevance not essential to the main invention found in the independent claims. Thus, a detailed discussion of the well known claim feature(s) is not warranted at this time. For example, claims 7 and 9 recite storages on separate or single chips. Placing circuit components on a single chip is advantageous for many reasons (improvements in speed and integration being just a few). Whereas, maintaining components on separately chips may be cheaper and easier to build. Because programming and/or erasing is a well known function performed by non-volatile memory devices for accurate and reliable storage, it would have been obvious to program and/or erase memory non-volatile memory as is customarily found in the prior art to reliably store and maintain data. Therefore, the claimed invention would have been obvious to one of ordinary skill in the art at the time of the invention.

**Any response to this action should be mailed to:**

Under Secretary of Commerce for Intellectual Property and
Director of the United States Patent and Trademark Office
PO Box 1450
Alexandria, VA 22313-1450

**or faxed to:**

(703) 872-9306, (for Official communications intended for entry)

**Or:**

(703) 872-9306, (for Non-Official or draft communications, please label "Non-Official" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack A. Lane whose telephone number is 703 305-3818. The examiner can normally be reached on Mon-Fri from 7:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703 306-2903.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-3900.

JACK A. LANE
PRIMARY EXAMINER